Electrical Properties of Si-based Junctions by SAB

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***Abstract*—Electrical properties of surface-activated-bonding (SAB) based Si/Si and Si/GaN junctions were investigated. Current-voltage (I-V) characteristics of n-Si/n-Si and n-Si/n-GaN junctions revealed ohmic features at room temperature. The p-Si/n-Si junctions showed asymmetric I-V characteristics, whose features were consistent with the scheme of the trap-assisted tunneling for the carrier transport across the interfaces. The I-V characteristics of respective Si/Si dice were close to one another and those of Si/GaN junctions were stable after measurements in varied temperatures. These results suggest that SAB is compatible with the standard semiconductor device process and potentially applicable to fabricating novel devices.**

***Keywords*—surface activated bonding, Si, GaN, current-voltage characteristics, trap-assisted tunneling, hybrid tandem solar cell**

I. Introduction

Heterostructures composed of III-V compound semiconductors and Si are attractive elements for innovative photovoltaic devices as well as for advanced electron and photonic devices [1], [2]. In intensive investigation on fabrication of III-V compound semiconductor layers on Si substrates, AlGaAs [3] and InGaP [4] layers on (100) Si substrates as well as group-III nitrides on (111) Si substrates [5] were applied for photovoltaic devices. Excellent performances of InGaP/InGaAs/Ge triple-junction tandem solar cells, which are photovoltaic devices composed of sub-cells whose bandgaps are different from each other, were reported [6].

The above cited structures were epitaxially grown on substrates, or formed in the monolithic approach. Heterostructures for the photovoltaic devices can also be fabricated in another process, or the hybrid approach:In this approach, semiconductor layers are bonded on substrates so that the heterostructures are synthesized. For example, n-GaAs and n-InP substrates were attached to each other by bonding for realizing hybrid tandem cells [7].

Heterostructures composed of materials with different crystal structures or different lattice constants might be fabricated possibly easily by using the hybrid approach. There still remains, however, an issue in this approach, which is related to the electrical properties at the interfaces between bonded materials. Actually it was reported that the electrical properties at interfaces depended on several factors such as treatment on surfaces of substrates prior to bonding, temperature while bonding and in subsequent annealing [8]. It was pointed out that the subsequent annealing at temperatures typically at 600 °C was essential for achieving interfaces with good electrical properties [7], [8]. Such high temperatures of samples might bring about another issue originating from the difference in thermal expansion coefficients of bonded materials. Methods for bonding at lower temperatures, consequently, are likely to be more preferable. Furthermore, the mechanical stability of interfaces as well as the uniformity of the electrical properties at interfaces, which are both essential from the practical viewpoints, is to be confirmed.

In this work the surface activated bonding (SAB) [9], which enables us to bond substrates to each other at around room temperature, is applied for fabricating Si-based junctions. We investigate their electrical properties by measuring the current-voltage (I-V) characteristics. Furthermore we discuss the uniformity of the electrical properties and the mechanical stability of junctions and explore the possibility of SAB process for realizing novel functional devices.

II. Experiments

A. Sample Preparation

We employed n- (P-doped) and p- (B-doped) (100) Si substrates as well as n- (Si-doped) GaN layers epitaxially-grown on sapphire substrates. Non-destructive measurements revealed that the resistivity and the carrier concentration of Si substrates were 0.02 Ωcm and $\sim 1 \times 10^{18}$ cm^{-3} (n-Si) and 0.02 Ωcm and $\sim 5 \times 10^{18}$ cm^{-3} (p-Si), respectively. The carrier concentration in n-GaN layers was estimated to be $\sim 8 \times 10^{17}$ cm^{-3}. By using SAB and dicing we fabricated 2-mm by 2-mm dice of n-Si/n-Si and p-Si/n-Si junctions with metallization on their tops and bottoms. It is noteworthy that prior to bonding no procedure for removing native oxide layers on surfaces of Si substrates was utilized. The temperature of substrates was not intentionally raised while they were bonded. The in-plane directions of substrates were not precisely aligned with each other. We also fabricated n-Si/n-GaN junctions by bonding 15-mm by 15-mm n-Si substrates to the surface of GaN layers.

We observed cross-TEM (XTEM) images of interfaces in n-Si/n-Si and p-Si/n-Si junctions, which are shown in Figs. 1(a) and 1(b), respectively. The two images suggested that transient layers, which were assumed to be amorphous, were formed around interfaces of the respective samples, whose thicknesses were estimated to be 9 and 7.5 nm for n-Si/n-Si and p-Si/n-Si junctions, respectively. We also found that the misalignment

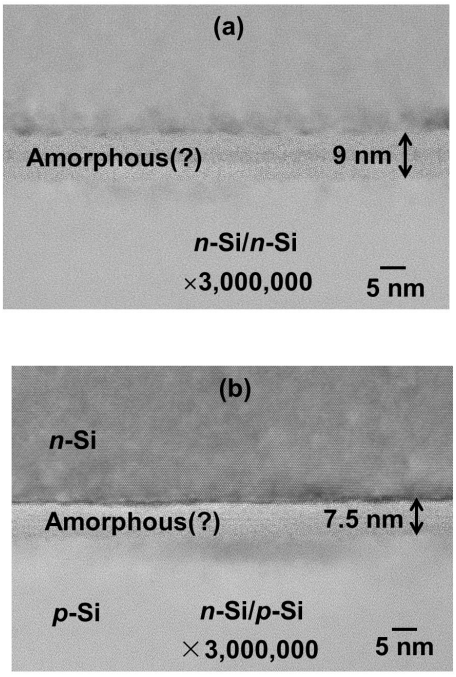

Fig. 1. Cross-TEM images of in (a) n-Si/n-Si and (b) p-Si/n-Si junctions.

of bonded Si substrates in the in-plane direction was $\approx 6^\circ$ in both n-Si/n-Si and p-Si/n-Si junctions by rotating the samples in XTEM observation. Furthermore, we performed the energy-dispersive X-ray spectroscopy analysis so that no oxide layers were observed around the interfaces (not depicted).

B. Current-Voltage Characterisitcs

1) n-Si/n-Si and n-Si/n-GaN junctions: The I-V characteristics of twenty n-Si/n-Si dice at room temperature are shown in Fig. 2(a). Influences of resistances at contacts and those inside of substrates were not compensated. I-V characteristics of the respective dice, which revealed ohmic features, were close to one another. In Fig. 2(b) is shown the I-V characteristics of one n-Si/n-Si die for several temperatures between -194 and 196°C. We found that ohmic features was retained for the entire range of temperatures although the resistance increased as the temperature decreased.

Figure 2(c) shows the I-V characteristics of n-Si/n-GaN junctions at varied temperatures between -189 and 196 °C. Ohmic features were dominant in the I-V characteristics at temperatures higher than room temperature although the I-V characteristics at temperatures below -101 °C revealed non-linear properties. We also confirmed that the n-Si substrate remained firmly bonded to the n-GaN layer after they had experienced the change in ambient temperature of $\sim \pm 200$°C.

2) p-Si/n-Si junctions: I-V characteristics for twenty p-Si/n-Si dice at room temperature are shown in Fig. 3(a). These curves were almost in agreement with one another. We found that the magnitude of the current for forward biases was larger than that for reverse biases as expected for conventional p-n junctions. Furthermore we found that the magnitude of the current gradually increased as the junctions were more deeply reverse-biased.

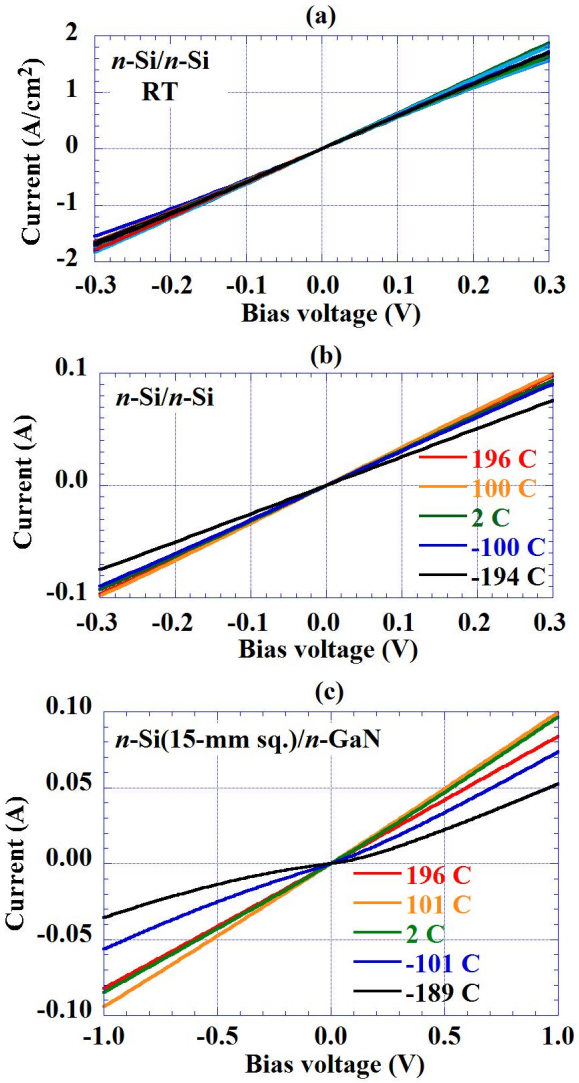

Fig. 2. (a) I-V characteristics of twenty n-Si/n-Si dice at room temperature. (b) I-V characteristics of one die at temperatures between -194 and 196 °C. (c) I-V characteristics of n-Si/n-GaN junctions at temperatures between -189 and 196 °C.

The I-V characteristics of one p-Si/n-Si die at temperatures between -190 and +199 °C are shown in Fig. 3(b). We found that the current for reverse-bias voltages increased and the turn-on voltage decreased as the temperature increased. The I-V characteristics for low forward-bias voltages (between 0.05 and 0.15 V) are shown in semi-logarithmic scales in Fig. 3(c). Straight lines for eyeguide and the extracted ideality factors for the data at the respective temperatures are also shown. The ideality factor was prohibitively larger (> 2) for lower temperatures, resulting from that the slope of the lines is almost independent of temperatures.

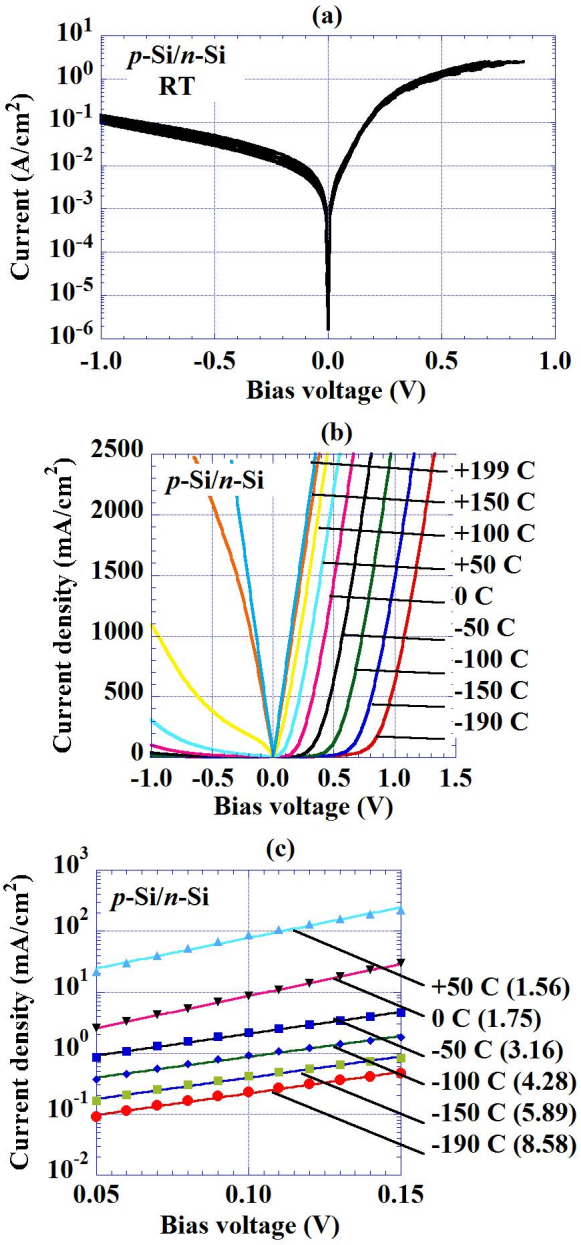

Fig. 3. (a) I-V characteristics of twenty p-Si/n-Si dice at room temperature. (b) I-V characteristics of one p-Si/n-Si die at temperatures between -190 and 199 °C. (c) I-V characteristics of one die for bias voltages between 0.05 and 0.15 V and the ideality factors at the respective temperatures.

III. Discussions

It is assumed that the amorphous-like layers formed at the interfaces of n-Si/n-Si junctions [Fig. 1(a)] should induce modulation in potential and might cause an influence on the transport properties of electrons across the interfaces, which is likely to be more marked in lower temperatures [8]. Given that ohmic properties were retained in the characteristics of n-Si/n-Si junctions for the entire range of temperatures for measurements [Fig. 2(b)], such possible influence of the amorphous-like layers is likely to be small from the practical viewpoint.

Amorphous-like layers are assumed to be formed at the Si/GaN interfaces similarly to the Si/Si interfaces. In addition, given that the electron affinity is estimated to be 4.05 and 3.4 eV for Si and GaN [10], respectively, a conduction-band discontinuity as large as $\sim$ 0.5 eV might occur at Si/GaN interfaces. The result that the I-V characteristics in the n-Si/n-GaN junctions revealed non-ohmic features for temperatures lower than -101 °C [Fig. 2(c)], consequently, suggests that the transport properties of electrons across the Si/GaN interfaces are deteriorated by either or both of these two factors. We have to note, however, that the measured I-V characteristics are likely to be under the influence of the sheet resistance, or spread resistance, in GaN layers, since the GaN layers grown on sapphire substrates were employed. Usage of GaN layers with a larger carrier concentration and/or those grown on conductive substrates are essential for more precise discussion.

The features observed in I-V characteristics of forward-biased p-Si/n-Si junctions that (i) the turn-on voltage was lowered for higher temperatures [Fig. 3(b)] and (ii) the slope in current was almost invariant to temperatures indicating that the ideality factor was > 2 in lower temperatures [Fig. 3(c)] are the same as those reported for p-GaAs/n-GaN junctions obtained by the wafer fusion process. In the latter junctions the tunneling had been assumed to be the dominant mechanism of the carrier transport [11].

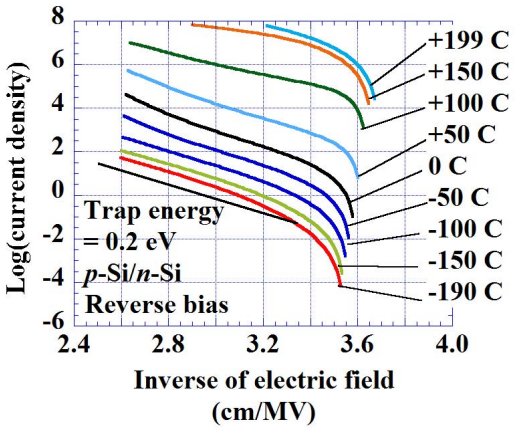

Fig. 4. The dependencies of currents for reverse-bias voltages on the inverse of averaged electric fields in depletion regions of one p-Si/n-Si die at varied temperatures. A line on the trap-assisted-tunneling model is also shown.

We consequently adopted the trap-assisted tunneling model [12] for analyzing the I-V characteristics in the p-Si/n-Si junctions. Using this model, the current density $J_{\rm TAT}$ in the reverse-biased junctions is assumed to be given by

$$J_{\rm TAT} = A_{\rm TAT}\exp(-\frac{8\pi\sqrt{2qm^*}}{3hE_{ave}}\phi_r^{1.5}), \qquad (1)$$

where h is the Planck constant, q is the elementary electric charge, m^* and ϕ_r are the effective mass of tunneling carriers and the energy level of traps dominating the tunneling process, respectively. The averaged electric field in the depletion region

E_{ave} is given by

$$E_{ave} = \frac{\sqrt{(q/2\epsilon\epsilon_0)(V_{bi} - V_{appl})}}{\sqrt{1/N_{\rm A} + 1/N_{\rm D}}}, \quad (2)$$

where ϵ and ϵ_0 are the dielectric constant of Si (11.7) and the permittivity of vacuum, respectively. The applied bias voltage V_{appl} is negative when the junctions are reverse-biased and the built-in voltage V_{bi} is 1.12 V, or the bandgap of Si at room temperature divided by q. Note that the doping concentrations of n-Si substrates $N_{\rm D}$ ($\sim 1 \times 10^{18}$ cm^{-3}) and p-Si substrates $N_{\rm A}$ ($\sim 5 \times 10^{18}$ cm^{-3}) are small enough for effects of the degeneracy of carriers to be negligible in the first approximation.

Figure 4 shows dependencies of the current on $1/E_{ave}$ of the reverse-biased p-Si/n-Si junction. A line whose slope corresponds to $m^* = 0.36m_0$ [13] and $q\phi_r = 0.2$ eV is also shown for eyeguide. We find that irrespective of temperatures the dependence of the current on $1/E_{ave}$ agrees with this line in slope.

This result is consistent with the scheme that traps with typical depth of $\sim$ 0.2 eV were formed on the surfaces of Si substrates possibly when the surfaces were irradiated by Ar plasma in the SAB process so that the tunneling through these traps played a major role in the transport properties of carriers across the Si/Si interfaces. The influence of such traps might be relatively lowered when the probability of the band-to-band tunneling is enhanced by employing substrates with higher carrier concentrations on their surfaces.

The result that I-V characteristics of twenty 2-mm by 2-mm Si/Si dice (both n-Si/n-Si and p-Si/n-Si) were almost identical to one another [Figs. 2 (a) and 3(a)] suggests that the electrical properties of SAB-based Si/Si junctions were uniform. In addition, it is noteworthy that 15-mm by 15-mm Si chips were firmly bonded to GaN layers after they had experienced a thermal stress of $\pm$200 °C in spite of a difference in the thermal expansion coefficients between Si (2.6×10^{-6} /K) and GaN (3.1×10^{-6} /K) [14]. These results suggest that SAB is promising in terms of the compatibility with the standard semiconductor process.and potentially applicable for fabricating novel semiconductor devices such as tandem solar cells.

IV. Conclusion

We fabricated n-Si/n-Si, n-Si/n-GaN, and p-Si/n-Si junctions by surface activated bonding (SAB) and dicing and investigated their electrical properties. The current-voltage (I-V) characteristics of both of the n-Si/n-Si and n-Si/n-GaN junctions revealed ohmic features at room temperature. Measurements of the I-V characteristics of p-Si/n-Si junctions in varied temperatures brought about results consistent with the scheme of the trap-assisted tunneling across the interfaces. The results that the electrical properties of respecive Si/Si dice were close to one another and the Si/GaN junctions were mechanically stable after they had experienced a thermal stress of $\pm$200 °C suggested that SAB is compatible with the standard semiconductor device process and is potentially applicable for fabricating novel devices.

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